I input port mechanisms with a width, which receive packets from a communication line, where I is greater than or equal to 1 and is an integer;

O output port mechanisms with a width, which send packets to a communication line, where O is greater than or equal to 1 and is an integer;

a carrier mechanism for carrying packets, said carrier mechanism having a width wider than the width of the input and output port mechanisms, said carrier mechanism connected to each input port mechanism and each output port mechanism;

a memory mechanism in which packets are stored, said memory mechanism connected to the carrier mechanism; and

a mechanism for providing packets to the memory mechanism through the carrier mechanism from the input port mechanisms, said providing mechanism able to transfer packets or portions of packets whose total width equals the width of the carrier mechanism in each transfer cycle to the memory mechanism.

5. A system as described in Claim 4 wherein the providing mechanism also provides packets from the memory mechanism to the output port mechanisms through the

carrier mechanism, said providing mechanism transferring packets or portions of packets whose total data equals the width of the carrier mechanism in each transfer cycle from the memory mechanism.

15. A switching system for packets comprising:

a central resource having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource partitioned via time slots that are allocated to the input and output port mechanisms, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by the input or output port mechanisms width; and

a memory mechanism for storing packets, said memory mechanism connected to the central resource.